THERMAL MANAGEMENT IN THREE DIMENSIONAL NETWORK-ON-CHIP USING BIO-INSPIRED LIQUID CHANNEL PLACEMENT

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ABSTRACT

Three-dimensional Network-on-Chip systems are becoming popular because of reduced communication delay, heterogeneous integration of different technologies in a single chip, high yield, reduced latency, and less consumption of interconnect power. However, the addition of functional units in the Z-direction has resulted in higher on-chip temperature and appearance of hot spots on the die. Liquid channel cooling has emerged as an efficient and scalable solution for 3-D NoC. This paper proposed a placement strategy of liquid micro-channels in the chip using the genetic algorithm. The proposed liquid cooling approach is independent of any topology. By performing an extensive set of experiments, the result shows a substantial decrease in peak on-chip temperature.

Keywords: Network-on-Chip, Hotspot, Liquid Channel, Genetic Algorithm, Thermal management.

1 INTRODUCTION

The complexity of System-on-Chip (SoC) increases with continuous scaling in semiconductor technology. At such high level of integration, communication channels play a significant role for active communication among all functional units. Traditional buses can no longer meet the communication requirement for future SoCs because of poor scalability. Due to their inefficiency, shared buses are replaced by Network-on-Chip (NoC), which has risen as a promising on-chip architecture due to its adaptability, alleviated power consumption, fault tolerance, ease of use and higher throughput (Benini and De Micheli 2002, Jantsch, Tenhunen, et al. 2003, Bjerregaard and Mahadevan 2006).

3-D NoC is the combination of NoC and a 3-D integrated circuit (IC). The advantages of the systems based on network-on-chip include adaptability, consistency, and scalability. Also, they provide higher bandwidth channels for parallel communicating systems. One of the primary concern in the acceptance of three-dimensional architecture is the increase in power density that arises from the placement of one computational module over another in the 3-D stack.

In our paper, we have proposed a novel algorithm for optimal placement of liquid channels in different layers of the chip using the genetic algorithm. The major contributions of the paper are as follows:

1. Insertion of liquid micro-channels in the 3-D stacked homogeneous architecture.
2. Proposed a genetic algorithm formulation for placement of liquid channels in 3-D NoC architectures with temperature beyond the threshold.

The remaining part of the paper is arranged as follows: Section 2 carries out a literature review on thermal management techniques in 3-D NoC architectures. Our proposed liquid channel placement algorithm based on genetic algorithm is detailed in section 4. Section 5 discusses the thermal diagram, simulation results and analysis obtained for three different network-on-chip architectures. Finally, the conclusion part of the paper is given in section 6.

2 RELATED WORK

Liquid channel cooling technology is an emerging solution to eliminate the high temperature in 3-D NoC, because of efficient heat removal capability of liquid channels than air channels (Coskun, Atienza, Rosing, Brunschwiler, and Michel 2010). Micro-channels are inserted in different layers of a 3-D chip. Fluid is injected through micro-channels between the various layers of a 3-D NoC using a pump to alleviate peak on-chip temperature. The number of channels increases with the addition of more number of layers.

Generation of uncontrolled heat flux in 3D ICs is one of the most glaring issues in design of such ICs, which results in increasing power densities and peak temperatures across the layers(Lau and Yue 2009)(Puttaswamy and Loh 2006). Although there are several cooling techniques for 2D planar circuits such as loop heat pipe(Maydanik, Vershinin, Korukov, and Ochterbeck 2005), thermoelectric microcooler(Fan, Zeng, LaBounty, Bowers, Croke, Ahn, Huxtable, Majumdar, and Shakouri 2001), compact thermosyphon(Kim, Joshi, and Fedorov 2008), and miniature absorption heat pump(Pal, Joshi, Beitelmal, Patel, and Wenger 2002), these techniques do not directly map onto 3D stacked ICs. Liquid micro-channel cooling technique comes as a possible solution for thermal management in 3D ICs.

Among several researchers to have investigated cooling ICs using liquid channels, it was first discussed in (Tuckerman and Pease 1981). Since then, a lot of research has been carried out in this field, including studies into the feasibility of liquid channel cooling method(Lee, Jeong, Shin, Baek, Kang, and Chun 2004)(Bhunia, Boutros, and Chen 2004). Prototypes built by using the inter-layer liquid channels have exhibited high heat removal capacity (Brunschwiler, Michel, Rothuizen, Kloter, Wunderle, Oppermann, and Reichl 2009). A three-dimensional chip has been developed in IBM Zurich Research Laboratory, containing several micro-channels to allow the flow of liquid. The inter-layer chip width is $50\mu m$. It is able to cool at the rate 180 $watt/cm^2$, for a layer with area of $4cm^2$ (Gruener 2008).

Coskun et al. developed a thermal model for three-dimensional architectures using micro-channel liquid cooling (Coskun, Ayala, Atienza, and Rosing 2009) by using Hotspot thermal simulator (Huang, Ghosh, Velusamy, Sankaranarayanan, Skadron, and Stan 2006). Sridhar et al. developed the first thermal transient simulation for liquid-cooled circuits. Their simulator named 3D-ICE (Sridhar, Vincenzi, Ruggiero, Brunschwiler, and Atienza 2010) creates a resistor-capacitance or R-C circuit model for the micro-channels. Then

Table 1: **Geometric properties of the stack.**

Stack width	$12,0010\mu m$
Stack length	$10,5000\mu m$
Cell size $(L \times W)$	$300 \times 300\mu m$
Liquid channel width	$300\mu m$
SiO_2 height	$50\mu m$
Si height	$150\mu m$
Epoxy height	$25\mu m$

by integrating the newly generated R-C model with the existing one, it can perform conduction-convention experiments in circuits cooled by liquid micro-channels.

Cyber-physical thermal management approach with inter-tier cooling is proposed by Qian et al. (Qian, Huang, Yu, and Chang 2011). The process used here is software-based temperature estimation and prediction. The flow of liquid is non-uniform in various micro-channels according to the temperature of different modules. The thermal effect of inserting liquid channels in between active layers are analyzed in (Del Valle and Atienza 2011, Coskun, Ayala, Atienza, Rosing, and Leblebici 2009).

None of the above-discussed methods have considered the possible placement of liquid channels to alleviate the on-chip temperature. Our proposed approach involves two steps: First, the temperature of original 3-D NoC architecture is determined, and then, the genetic algorithm is applied to optimize the placement of liquid channels in different layers. The motivation behind the use of genetic algorithm to optimize the position of liquid micro-channels is that these micro-channels have certain disadvantages - high fabrication costs and high power consumption by a micro-channel (for pumping the coolant through the micro-channels). Therefore, we aim to use a limited number of liquid micro-channels to bring down these costs while maximizing their effect in cooling the 3D NoC. Exhaustive simulations show that our approach can decrease the on-chip temperature efficiently. The simulations also conclude that our approach provides better results than other floorplanning techniques to alleviate on-chip temperature.

3 MATHEMATICAL MODEL

In this section, we developed a mathematical model to calculate the temperature distribution throughout the 3D stack with the addition of liquid channels. The thermal model to calculate the temperature profile of the layers in the 3D chip is derived from Brook's equation.

The energy conservation equation for heat transfer in flowing liquids can be written in differential form is stated by equation 1 :

$$C_v \cdot \frac{\mathrm{d}T}{\mathrm{d}t} + \nabla \cdot (-k \cdot \nabla T) + C_v \cdot \overrightarrow{u} \cdot \nabla T = q \tag{1}$$

where T is the temperature of the control volume, k is the thermal conductivity of the material, q is the volumetric generation of heat inside the volume, C_v is the volumetric specific heat of the material, and $\overrightarrow{u}$ represents net outflow of the heat from the control volume due to convection.

Applying eight point finite difference discretization to equation 1 in order to perform numerical thermal analysis over the three dimensional volume of the NoC system. The NoC blocks are decomposed the into various rectangular blocks of different shapes and sizes. Diffusion of heat occurs among these blocks. Now, each block is characterized by its power dissipation, initial temperature, thermal capacitance and thermal

resistance to adjacent elements. At an inner point of the chip element, the discretization equation is given as follows:

$$\begin{aligned}\rho cv\frac{T_{i,j,l}^{q+1}}{\triangle t} &= -2.\left(g_x+g_y+g_z\right).T_{i,j,l}^{q}+g_x.T_{i-1,j,l}^{q}\\ +g_x.T_{i+1,j,l}^{q}+g_y.T_{i-1,j-1,l}^{q}&+g_x.T_{i,j+1,l}^{q}+g_z.T_{i,j,l-1}^{q}\\ &+g_z.T_{i,j,l+1}^{q}+V.p_{i,j,i}\end{aligned} \tag{2}$$

where, i, j and l are discrete offsets along the X, Y and Z axes, respectively, ρc is known as volumetric specific heat of material, $\triangle t$ is the discretization step in time t. $\triangle x$, $\triangle y$ and $\triangle z$ are discretization steps along the X, Y and Z axes respectively, V= $\triangle x \times \triangle y \times \triangle z$. Finally, g_x, g_y and g_z are the thermal conductivities between adjacent elements. These are defined as follows:

$$\begin{aligned}g_x &= k\left(\triangle y.\triangle z/\triangle x\right)\\ g_y &= k\left(\triangle x.\triangle z/\triangle y\right)\\ g_z &= k\left(\triangle x.\triangle y/\triangle z\right)\end{aligned} \tag{3}$$

4 LIQUID CHANNEL INSERTION ALGORITHM

This paper analyzes the effect of liquid channel placement using genetic algorithm on the maximum temperature of various layers in a 3-D NoC. The proposed algorithm places the coded solutions that are iteratively improved in the process of genetic evolution to provide a thermal-aware architecture. In this work, LC_{NoC} simultaneously optimizes the following two objectives:

- O_1: The first objective takes into account the number of topological constraints violated while placing the liquid channels in the chip. Violation of topological constraints means the overlapping between different liquid channels, or placement of liquid channels outside the periphery of the chip.
- O_2: Minimization of the on-chip peak temperature: On-chip temperature is dependent upon the thermal model used. In the case of our proposed algorithm, LC_{NoC}, the maximum temperature generation of two blocks i and j depends upon the cross product of their power densities. Peak temperature is different at each layer. Our algorithm optimizes the placement of liquid channels according to the peak temperature value to minimize the peak temperature.

The input is given in the form of maximum number of layers, topological values of each functional unit number of liquid channels, and power consumption of all the blocks. By taking all the discussed input into account, an incremental floorplanning is carried out. The floorplanning method is constructive in nature, i.e. the process will start from a seed module, and it will go on adding more number of modules to the die until all the remaining blocks are added to the die. After the process is complete, the original floorplan is generated. Then, a heuristic is used to place the liquid channels according to the peak temperature value in different layers. The genetic operators i.e. selection, crossover, and mutation are applied to the floorplan to get a set of floorplans according to the decreasing order of their fitness function. The floorplan with the highest value of fitness function is chosen, and the thermal simulator is run with the optimized floorplan as an input to get the maximum temperature of each layer. The resulting thermal diagrams are generated at this stage.

Algorithm 1 *Optimal Liquid Channel Placement Algorithm for 3D NoC*

```
 1: procedure PLACELC()
 2:     generate initial Population
 3:     evaluate(Population)
 4:     set bestIndividual ← bestOf(Population)
 5:     while not stopCriteria do
 6:         newPopulation ← ϕ
 7:         for j = 1 to M/2 do
 8:             select p1 and p2 from Population
 9:             crossover(p1, p2, c1, c2)
10:             Add c1 and c2 to newPopulation
11:         end for
12:         evaluate(Population ∪ newPopulation)
13:         Population ← reduce(Population ∪ newPopulation)
14:         for j = 1 to M do
15:             mutate(Population[j], P_M)
16:             invert(Population[j], P_I)
17:         end for
18:         evaluate(Popualtion)
19:         bestIndividual ← bestOf(Population ∪ bestIndividual)
20:     end while
21:     optimize(bestIndividual)
22:     return bestIndividual
23: end procedure
```

Algorithm 1 describes the evolutionary approach to achieve optimal placement of liquid micro-channels in 3D NoCs. Beginning with a random set of solutions (*Population*), the heuristic approach outlined continuously evaluates and improves the solutions for a number of iterations. The iteration is ceased when either the best possible solution is reached or a predefined number of generations have been generated. Various genetic operators, namely *selection*, *crossover*, *mutation*, and *inversion* are used to improve the solutions. The evaluation function is used to determine the fitness of a given solution and is taken from (Cuesta, Risco-Martín, Ayala, and Hidalgo 2015). Finally, the best solution (individual with the best fitness from the population) is selected and returned as the optimized solution.

The *evaluate* procedure used in Algorithm 1 takes a set of solutions as its input parameter and calculates the fitness of each of the solutions as described in (Cuesta, Risco-Martín, Ayala, and Hidalgo 2015). The function goes on to calculate the expected temperatures after inserting the liquid micro-channels. It should be noted here that the liquid micro-channel may not be inserted directly at the hotspots (coordinates with temperatures above an acceptable threshold) but at such places where the overall cooling effect of all the micro-channels considered together is the best. Moreover, for a given 3D NoC, we have simulated the placement of an average of five micro-channels for each layer(Cuesta, Risco-Martín, Ayala, and Hidalgo 2015). The algorithm proposed optimizes the placement as well as the number of liquid micro-channels for every layer of the 3D NoC and thus, an optimal solution may have more than five micro-channels in one layer while less than five in another.

5 EXPERIMENTAL SET-UP AND RESULTS

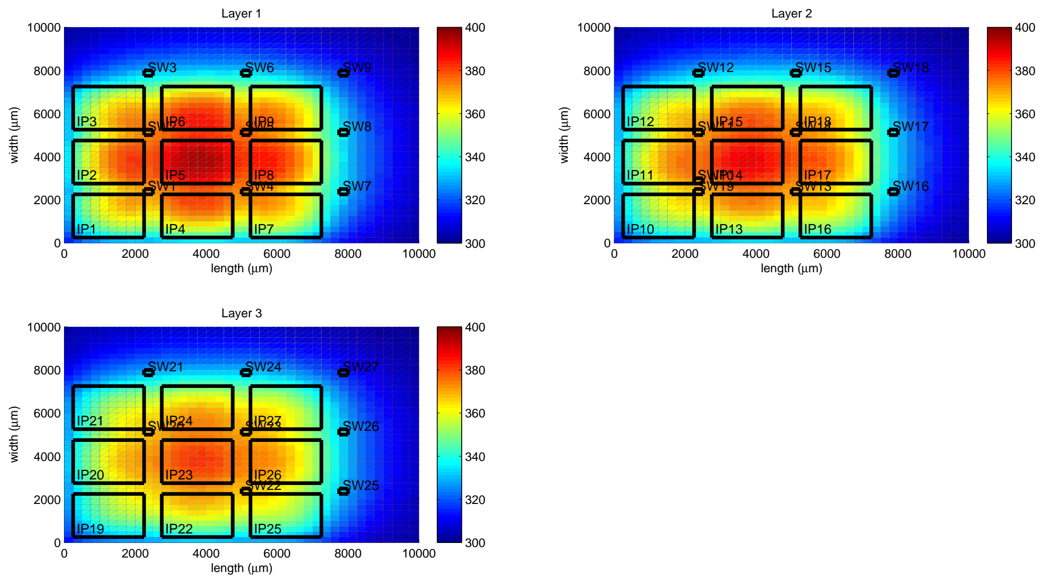
The mathematical model of the proposed optimization method has been validated with the 3-D ICE thermal simulator (Sridhar, Vincenzi, Ruggiero, Brunschwiler, and Atienza 2010). Our experiments have been run in an Intel Core i7-6785R Processor @3.90GHz. For the initial placement algorithm, the population is set to 100 individuals, which has been proven to be a sufficient population to find feasible solutions. The algorithm is also configured using a probability of the crossover is 0.90. The probability of the mutations is set to 1/number of functional blocks, and the maximum number of generations is set to be 2500. These parameters have been set using the guidelines recommended in (Deb, Pratap, Agarwal, and Meyarivan 2002). The best suitable position of a liquid channel is based on the temperature of that layer. If the temperature is high, the liquid channels are placed nearer to each other; else they can be placed far. Then, as described in Algorithm 1, the genetic algorithm operators are applied to achieve an optimized thermally balanced floorplan.

The system size assumed in this work is taken from (Feero and Pande 2009). We have considered a three-dimensional stacked 3-D mesh NoC architecture with $400mm^2$ floor-plan and 54 functional IP blocks as the base floor-plan. IP blocks for 3D SoC are mapped onto three $10mm \times 10mm$ layers in the base three layer floor-plan. The geometric properties of the functional units are given in Table 1. In the patterns shown in the Figures, space is dedicated to routing and communication units. Since the work is focused on the thermal impact of the distribution, these communication units are not considered in the description for their negligible thermal impact.

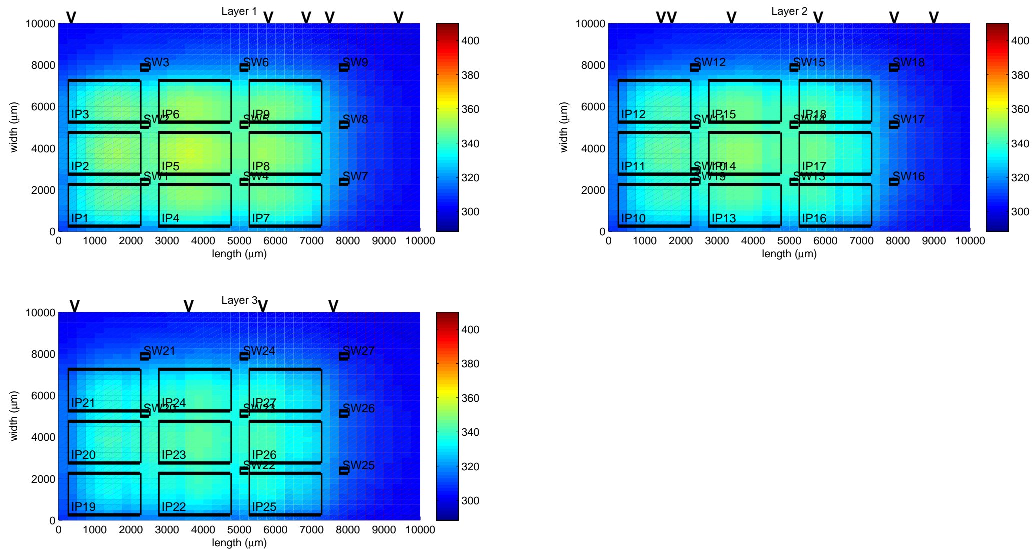
Table 2: Peak and Reduced Temperature per Layer in Homogeneous 3-D Stacked Network-on-Chip before and after placement of optimized liquid channels

Architecture	**Layer Number**	**Original Temperature** (in K)	**Resultant Temperature** (in K)	**Temperature Reduction** (in K)
3layer	1st	381.013	345.4013	25.6117
	2nd	387.2342	350.6764	36.5578
	3rd	393.9507	356.9937	36.9570
4layer	1st	398.5079	347.6092	50.8987
	2nd	406.0838	352.1988	53.8850
	3rd	415.0838	362.7751	52.3087
	4th	423.6995	369.6190	54.0805
5layer	1st	411.5411	348.8714	62.6697
	2nd	420.2010	355.3757	64.8253
	3rd	430.7982	363.7626	67.0356
	4th	443.8383	378.4185	65.4198
	5th	453.5233	385.8260	67.6973

The peak temperature of each layer is considered as the parameter to compare between the original and the floorplan with the liquid channel. The power values have been obtained from (Feero and Pande 2009). The number of functional unit in each layer is same for all the architecture considered. Figures 1, 2 and 3 represent the original and optimized thermal maps for each individual layer for the 3D homogeneous mesh NoC architecture for three-layer, four-layer and five-layer NoC architectures, respectively. The position of liquid micro-channels in the layers of the 3D NoC is indicated using 'V' symbol in Figures 1b, 2b and 3b. The maximum temperature of each distinct layer is obtained from the thermal simulator. The peak temperature of each layer in the original floorplan is compared with the peak temperature of the resultant floorplan after applying genetic algorithm operators for liquid channel placement. The equivalence with the original floorplan affirms that the floor planner can optimize the peak temperature in 48.5494K for three layers, in 76.0930K for four layers, and in 104.6519K for five layers homogeneous 3-D stacked NoC



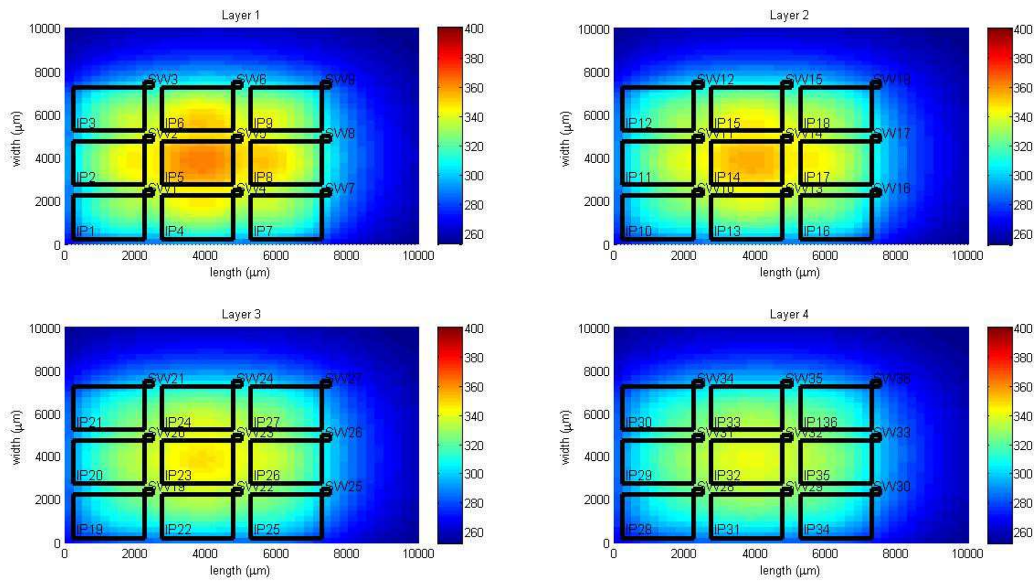
(a) Thermal map of original 3 layer homogeneous floorplan



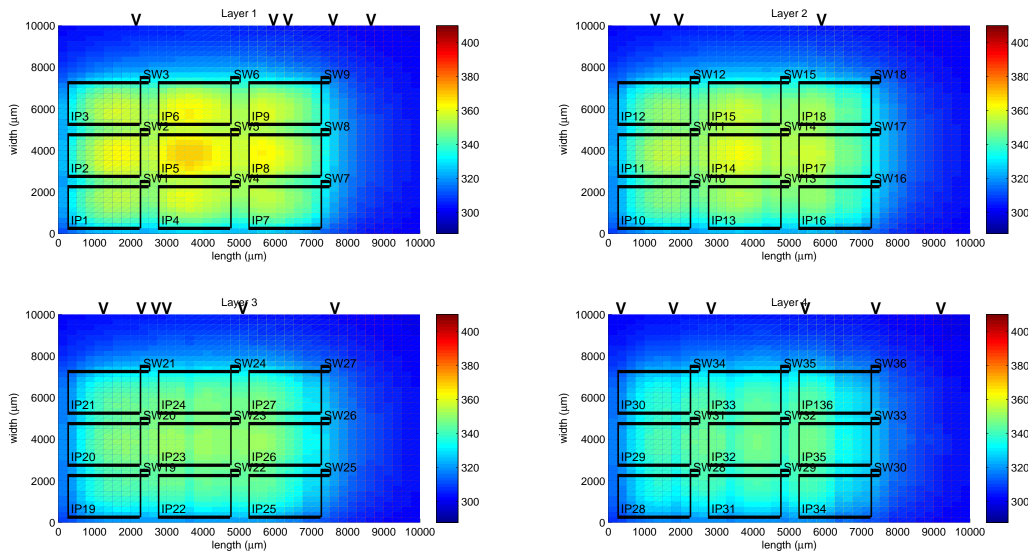
(b) Thermal map of 3 layer homogeneous floorplan after applying MOEA

Figure 1: Original and optimized thermal diagram of 3 layer homogeneous stacked 3D mesh based NoC

architecture in the best case. The experimental values have been provided in Table 2; table entries with peak temperatures greater than a threshold (in this case, 400 K) have been highlighted. The table clearly indicates the reduction in temperature after the use of genetic algorithm operators for liquid micro-channel placement. This decrease in temperature leads to a more uniform thermal distribution. It lowers the risk associated with reliability and reduces leakage current.



(a) Thermal map of original 3 layer homogeneous floorplan

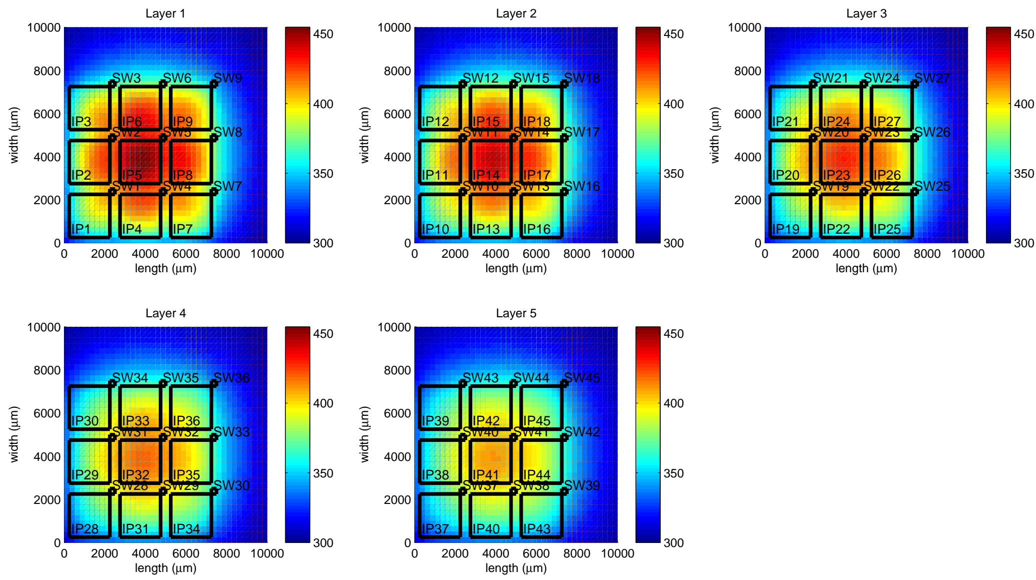


(b) Thermal map of 3 layer homogeneous floorplan after applying MOEA

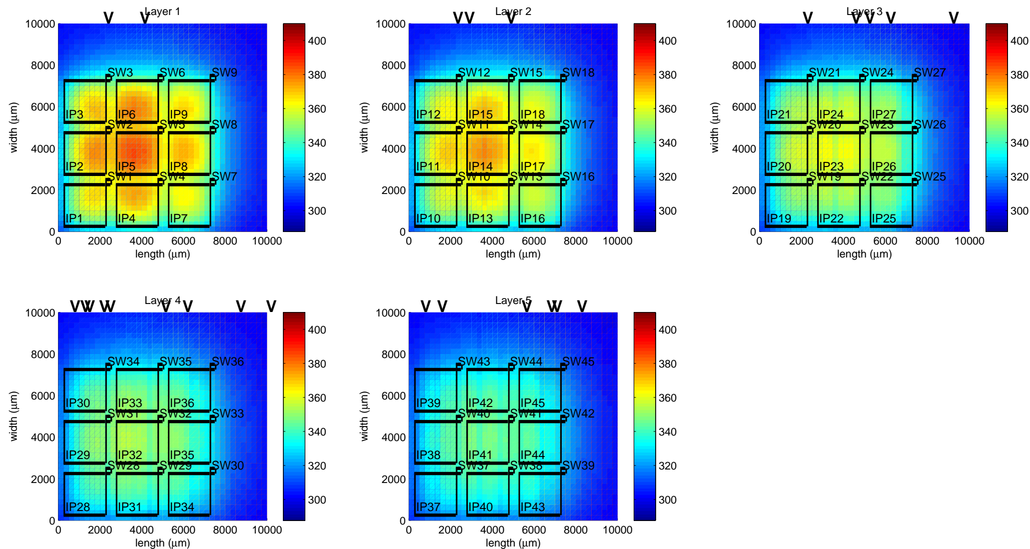
Figure 2: Original and optimized thermal diagram of 3 layer homogeneous stacked 3D mesh based NoC

6 CONCLUSION

In this paper, we have proposed a thermal management method by optimizing the position of liquid channels in different layers in case of a 3-D NoC architecture. Our thermal management method optimizes the placement of the liquid micro-channels for a given layer as well as between multiple layers. We perform this thermal management technique using the genetic algorithm. Based on the experimental results, we compared the peak temperature of the original design (3D NoCs without the liquid micro-channels) and the



(a) Thermal map of original 3 layer homogeneous floorplan



(b) Thermal map of 3 layer homogeneous floorplan after applying MOEA

Figure 3: Original and optimized thermal diagram of 3 layer homogeneous stacked 3D mesh based NoC

peak temperature of the same architecture with liquid micro-channels. The results demonstrate a substantial reduction in peak on-chip temperatures across all the layers. Thus, a practical implementation of our simulations will improve the reliability and longevity of 3D on-chip systems.

Even though our approach is novel and better than the rest of the floorplanning, we could further improve our results by using a hybrid approach - integrating both floorplanning and liquid micro-channels insertion.

Moreover, we could also consider routing in 3D NoCs and observe how effective is our approach and the hybrid approach when we involve routing in simulations.

REFERENCES

Benini, L., and G. De Micheli. 2002. “Networks on Chips: A New SoC Paradigm”. *computer* vol. 35 (1), pp. 70–78.

Bhunia, A., K. Boutros, and C.-L. Chen. 2004. “High heat flux cooling solutions for thermal management of high power density gallium nitride HEMT”. In *Thermal and Thermomechanical Phenomena in Electronic Systems, 2004. ITHERM’04. The Ninth Intersociety Conference on*, Volume 2, pp. 75–81. IEEE.

Bjerregaard, T., and S. Mahadevan. 2006. “A Survey of Research and Practices of Network-on-Chip”. *ACM Computing Surveys (CSUR)* vol. 38 (1), pp. 1.

Brunschwiler, T., B. Michel, H. Rothuizen, U. Kloter, B. Wunderle, H. Oppermann, and H. Reichl. 2009. “Interlayer Cooling Potential in Vertically Integrated Packages”. *Microsystem Technologies* vol. 15 (1), pp. 57–74.

Coskun, A. K., D. Atienza, T. S. Rosing, T. Brunschwiler, and B. Michel. 2010. “Energy-efficient Variable-flow Liquid Cooling in 3D Stacked Architectures”. In *2010 Design, Automation & Test in Europe Conference & Exhibition (DATE 2010)*, pp. 111–116. IEEE.

Coskun, A. K., J. L. Ayala, D. Atienza, and T. S. Rosing. 2009. “Modeling and dynamic management of 3D multicore systems with liquid cooling”. In *2009 17th IFIP International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 35–40. IEEE.

Coskun, A. K., J. L. Ayala, D. Atienza, T. S. Rosing, and Y. Leblebici. 2009. “Dynamic thermal management in 3D multicore architectures”. In *2009 Design, Automation & Test in Europe Conference & Exhibition*, pp. 1410–1415. IEEE.

Cuesta, D., J. L. Risco-Martín, J. L. Ayala, and J. I. Hidalgo. 2015. “Thermal-aware floorplanner for 3D IC, including TSVs, liquid microchannels and thermal domains optimization”. *Applied Soft Computing* vol. 34, pp. 164–177.

Deb, K., A. Pratap, S. Agarwal, and T. Meyarivan. 2002. “A fast and elitist multiobjective genetic algorithm: NSGA-II”. *Evolutionary Computation, IEEE Transactions on* vol. 6 (2), pp. 182–197.

Del Valle, P. G., and D. Atienza. 2011. “Emulation-based transient thermal modeling of 2D/3D systems-on-chip with active cooling”. *Microelectronics Journal* vol. 42 (4), pp. 564–571.

Fan, X., G. Zeng, C. LaBounty, J. E. Bowers, E. Croke, C. C. Ahn, S. Huxtable, A. Majumdar, and A. Shakouri. 2001. “SiGeC/Si superlattice microcoolers”. *Applied Physics Letters* vol. 78 (11), pp. 1580–1582.

Feero, B. S., and P. P. Pande. 2009. “Networks-on-chip in a three-dimensional environment: A performance evaluation”. *IEEE Transactions on Computers* vol. 58 (1), pp. 32–45.

Gruener, W 2008. “IBM Cools 3D Chips With Integrated Water Channels”.

Huang, W., S. Ghosh, S. Velusamy, K. Sankaranarayanan, K. Skadron, and M. R. Stan. 2006. “HotSpot: A compact thermal modeling methodology for early-stage VLSI design”. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* vol. 14 (5), pp. 501–513.

Jantsch, A., H. Tenhunen et al. 2003. *Networks on Chip*, Volume 38. Springer.

Kim, Y. J., Y. K. Joshi, and A. G. Fedorov. 2008. “An absorption based miniature heat pump system for electronics cooling”. *International Journal of Refrigeration* vol. 31 (1), pp. 23–33.

Lau, J. H., and T. G. Yue. 2009. "Thermal management of 3D IC integration with TSV (through silicon via)". In *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, pp. 635–640. IEEE.

Lee, H., Y. Jeong, J. Shin, J. Baek, M. Kang, and K. Chun. 2004. "Package embedded heat exchanger for stacked multi-chip module". *Sensors and Actuators A: Physical* vol. 114 (2), pp. 204–211.

Maydanik, Y. F., S. V. Vershinin, M. A. Korukov, and J. M. Ochterbeck. 2005. "Miniature loop heat pipes-a promising means for cooling electronics". *IEEE Transactions on Components and Packaging Technologies* vol. 28 (2), pp. 290–296.

Pal, A., Y. K. Joshi, M. H. Beitelmal, C. D. Patel, and T. M. Wenger. 2002. "Design and performance evaluation of a compact thermosyphon". *IEEE Transactions on Components and Packaging Technologies* vol. 25 (4), pp. 601–607.

Puttaswamy, K., and G. H. Loh. 2006. "Thermal analysis of a 3D die-stacked high-performance microprocessor". In *Proceedings of the 16th ACM Great Lakes symposium on VLSI*, pp. 19–24. ACM.

Qian, H., X. Huang, H. Yu, and C. H. Chang. 2011. "Cyber-physical thermal management of 3D multi-core cache-processor system with microfluidic cooling". *Journal of Low Power Electronics* vol. 7 (1), pp. 110–121.

Sridhar, A., A. Vincenzi, M. Ruggiero, T. Brunschwiler, and D. Atienza. 2010. "3D-ICE: Fast compact transient thermal modeling for 3D ICs with inter-tier liquid cooling". In *Proceedings of the International Conference on Computer-Aided Design*, pp. 463–470. IEEE Press.

Tuckerman, D. B., and R. Pease. 1981. "High-performance heat sinking for VLSI". *IEEE Electron device letters* vol. 2 (5), pp. 126–129.

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