SOLECTRON FIELD EFFECT TRANSISTOR AND INVERTER

1 Background

It is desirable that computers, including mobile phones and consumer electronic communication and computing devices, work with as low as possible energy consumption. This would help reduce the heat production problem in computers, and the relatively low lifetime of battery operated mobile phones. The present invention can reduce the energy consumption of computing.

2 Statement of invention

The invention proposes using solectrons as the current carriers in the source – drain channel of the field effect transistor.

3 Advantages

The first advantage of solectrons is that they are travelling at an almost constant velocity along the channel, independent of the source – drain voltage, for voltages greater than (kT/e), which is 25 mV at room temperature. For voltages greater than this the source – drain current is almost constant. Thus circuits such as the inverter can be operated at very low supply voltages. So also can circuits that rely on the inverter such as the Boolean logic gates used in computers.

The second advantage is that the gate – channel insulator thickness can be large, in comparison to the silicon field effect transistor. For in the latter the insulator thickness is constrained to be increasingly small as both the supply voltage and hence the threshold voltage, are reduced. A larger insulator thickness is desirable as it leads to a smaller gate input capacity, and so less energy consumption on switching. It also allows operation at smaller currents, leading to lower quiescent energy consumption.

The energy cost of an inverter switch scales proportionally to the square of the supply voltage, and inversely proportional to the gate insulator thickness. Thus, use of the two above advantages can lead to a much lower energy consumption using the present invention, compared to current silicon technology.

4 Introduction to drawings

The invention will now be described with reference to the accompanying drawings in which

Figure 1 illustrates the construction of the solectron field effect transistor.

Figure 2 illustrates an alternative construction of the solectron field effect transistor.

Figure 3 is a graph of the source–drain current as a function of the source-drain voltage.

Figure 4 is a graph of the source–drain current as a function of the gate–source voltage.

Figure 5 is the circuit diagram of the inverter made up of two solectron field effect transistors.

Figure 6 is a graph of the inverter transfer function for a supply voltage of 1000 millivolts.

Figure 7 is a graph of the inverter transfer function for a supply voltage of 200 millivolts.

Figure 8 is a graph of the inverter transfer function for a supply voltage of 100 millivolts.

5 Detailed description

5.1 What is a solectron ?

In a one dimensional insulator a lattice distortion and an extra electron (or hole) can form a coherent particle, a solectron. As for the classical polaron, the electron and lattice distortion move together. However, a characteristic of solectron motion is that the velocity is almost constant, independent of an applied electric field, even in a zero field, and of velocity around the sound velocity. One theoretical approach describes the solectron existing in a linear or nonlinear lattice, where the electron distorts the lattice, and the distortion holds the electron. [1], [2], [3]. Another theoretical approach describes a localized purely lattice deformation in a non linear lattice which traps or surfs any itinerant electron to form the solectron [4]. In reality both trapping mechanisms are expected to work together [5].

Solectrons in thermal equilibrium are moving at close to the sound velocity.

[1] A S Davydov (1991) "Solitons in Molecular Systems", Reidel, Dordrecht

[2] E G Wilson (1983) J Phys C: Solid State Phys **16** 6793

[3] O G Cantu-Ros, L Cruzeiro, M G Velarde and W Ebeling (2011) Eur Phys J B **80** 545

[4] M G Velarde (2010) J. Comput Appl Maths 233 1432

[5] M G Velarde, A P Chetverikov, W Ebeling, E G Wilson and K J Donovan (2014) EPL **106** 27004

The solectron has been seen experimentally in PDATS, (the toluene sulphonate derivative of polydiacetylene) which is a highly crystalline conjugated polymer comprised of conjugated carbon chains, perfectly parallel, and separated from each other by a distance large compared to electron wave function overlap [6]. Thus, each chain is an ideal one dimensional electronic system capable of supporting the solectron. A charge carrier was found which moved at a velocity of close to the sound velocity, unchanged when the electric field was varied by four orders of magnitude. The velocity was measured for fields from 10^2 to 10^6 volts per meter, and was constant. The solectron travelled almost mm distance before trapping, transiently, at some defect. [7]. This reflects the purity and perfection of the polymer chains.

[6] G Wegner (1971) Die Makromolekulare Chemie **145** 85

[7] K J Donovan and E G Wilson (1981) Phil Mag B **44**, 9.

5.2 The Solectron Field Effect Transistor (SFET)

The present invention uses the solectron as the charge carrier in the field effect transistor (FET) channel between source and drain.

The SFET will now be described by an example, using the PDATS crystal as the solectron supporting material.

The example to be given uses an electron solectron. However, the description, with obvious amendments, can be used for the hole solectron.

In Figure 1 metallic source electrodes 2 and 3 are evaporated onto the surface of the PDATS crystal 1, using appropriate masks to create the desired metal shapes. The polymer chains of the PDATS are oriented along the channel. An insulator layer 4 is then evaporated or spin coated, followed by a further evaporated or spin coated layer 5. Finally the gate metal 6 is evaporated.

The source, drain and gate metals are identical and chosen to have a lower work function than the PDATS electron affinity. Work functions of metals are known; as also is the electron affinity (and ionization potential) of PDATS. Thus, the source and drain metals, in thermal equilibrium, inject electrons into the conduction band of the PDATS. The gate metal also injects electrons into the layer 5.

Figure 3 shows a graph of the source – drain current, I_{SD} , along the axis 8, against the source – drain voltage, V_{SD} , along the axis 9. The current is denoted by the solid line 10. The point 11 denotes the voltage V_T which is (kT/e) = 25 mV. For $V_{SD} > V_T$ the current is carried by solectrons moving from source to drain at constant velocity. The voltage along the channel does not change. The solectron density along the channel does not change. For $V_{SD} < V_T$ the current falls, as solectrons of thermal energy under the drain can enter the channel and reach the source. Continuing increase of $V_{SD} > V_T$ does not change the channel voltage; or current; rather, a voltage fall, in a small length adjacent to the drain is increased in value.

Figure 4 shows a graph of the source – drain current, I_{SD} , along the axis 12, against the source – gate voltage, V_{SG} , along the axis 13. The current is denoted by the solid line 14 . The point 15 denotes a threshold voltage, V_{TH} . The point 16 denotes a voltage which is V_T greater than the threshold voltage. The threshold voltage is given by Equation (1),

$$V_{TH} = A_{PDA} - A_5 - V_T \qquad \text{Equation (1)}$$

where

A_{PDA} is the electron affinity of the PDATS labeled 1 on Figure1, and

A_5 is the electron affinity of the material of layer 5 on Figure 1..

Equation (1) accounts for the two different contact potentials at the interfaces of the metal and either the PDATS or the layer 5. The solectrons in the channel are at a voltage which is V_T less than the voltage in the PDA under the source; this is accounted for also in Equation (1). When the voltage V_{SG} is reduced to be within V_T of the threshold voltage, then the current ceases to fall linearly to zero, but falls more slowly, as solectrons of greater thermal energies than eV_T under the source, are able to enter the channel and reduce the voltage in the channel.

Figure 2 shows a further alternative embodiment showing a SFET constructed on flat insulating substrate 7. The gate metal 6, layer 5, insulating layer 4, and source and drain metal are successively formed on the substrate. The PDATS of the solectron channel is then made by polymerization of TS monomer crystal grown in situ as a further step in the construction process. It is well established how such polymerization can be done by heat or ultra violet or electron beam radiation. Means to orient the monomer crystal, such as use of a seed crystal, is required to orient the resulting polymer chains in the desired direction from source to drain.

It is necessary that the source – drain distance be sufficiently small, and the PDATS sufficiently pure, that solectrons travel from source to drain without trapping at impurities or defects.

5.3 Response time of the SFET

The limit to the response time of the SFET is the transit time, T, from source to drain. For example, for a solectron velocity such as in PDATS, $v = 2 \times 10^3$ m/s, and a source – drain distance of $L = 1$ μm, then

$$T = L/v \qquad \text{Equation (2)}$$

$$= 0.5 \text{ ns}$$

5.4 Input capacity of gate

The capacity between gate and channel, *C*, depends on the gate area, which for a SFET of width *W* cannot be smaller than *WL*. *C* also depends on the dielectric constants of the layers between gate and channel, ε, (taken for simplicity to be the same for both layers), and the distance from gate to channel, *d*, according to

$C = \varepsilon\varepsilon_0 WL/d$ Equation (3)

The distance *d* is constrained only by being of order *L* or less. This contrasts to the silicon FET in which the distance *d* is very severely constrained to a small value by the necessity of keeping the threshold voltage at a controlled and small value.

5.5 Output resistance

For source drain – drain voltages larger than V_T = 25 mV the output resistance for feeding a load connected to the drain is very low; the load current is almost independent of the drain voltage. This is a desirable property for many analogue circuit systems.

5.6 Transfer Impedance

The transfer impedance *Z* is defined here as the change of source - drain current in response to change of the gate – source voltage, ie

$Z = (dI_{SD}/dV_{SG}) = C/T = \varepsilon\varepsilon_0 \text{ v } (W/d)$ Equation (4)

which is valid for the source – gate voltage more than V_T above the threshold voltage. Thus, *Z* is dependent on only *W* and *d* and independent of *L*.

5.7 Threshold control

Equation (1) shows how the threshold voltage can be controlled by the choice of electron affinity of layer 5. Thus, a material constant, ie electron affinity, is used to determine the threshold voltage. This is in contrast to the silicon FET where the threshold is determined by the dopants.

There are many soluble PDA which can be spin coated to form thin films. These are candidates for use as layer 5, and will have similar electron affinities to the PDATS crystal. This layer is not required to be long chain perfect crystal, nor to support solectrons, but merely to be of desired electron affinity.

5.8 Inverter

The inverter, created from two SFET is described using Figure 5. 17 and 18 are the SFET, denoted α, and β respectively. The gate and drain of the βSFET are connected together. The input voltage, V_{in} , is applied at point 20, and the output voltage , V_{out} ,taken at point 21. The input capacity, *C*, of the next stage to be driven by the inverter, considered to be a further inverter, is labeled 19. The power supply voltage, *VDD*, is applied at point labeled 22. The universal ground symbol is used in Figure 5, and all voltages are with respect to that ground at zero voltage.

The transfer function, which gives the inverter output as a function of the input, is determined by the individual SFET characteristics of Figures 3 and 4. They are assumed identical, except that they can be of different width. So the transfer impedance of each SFET can be controlled. The characteristics of the SFET shown in Figures 3 and 4 can be expressed by Equation's (5), (6), (7) and (8). These equations, as well as Figures 3 and 4, are simplified abstractions of the SFET behavior. They nevertheless contain all the essential SFET properties, and are able to describe the behavior and limitations in electronic circuits.

$$I_{SD} = Z(V_{SG} - V_{TH}) \qquad V_{SG} > V_{TH} + V_T \qquad V_{SD} > V_T \qquad \text{Equation (5)}$$

$$I_{SD} = Z(V_{SG} - V_{TH})(V_D / V_T) \qquad V_{SG} > V_{TH} + V_T \qquad V_{SD} < V_T \qquad \text{Equation (6)}$$

$$I_{SD} = ZV_T \qquad V_{SG} < V_{TH} + V_T \qquad V_{SD} > V_T \qquad \text{Equation (7)}$$

$$I_{SD} = ZV_{SD} \qquad V_{SG} < V_{TH} + V_T \qquad V_{SD} < V_T \qquad \text{Equation (8)}$$

The inverter response is first considered in the case that both SFET are described by Equation (5). With reference to Figure 5 then

$$I_{SD\alpha} = Z_\alpha (V_{in} - V_{TH}) = I_{SD\beta} = Z_\beta (VDD - V_{out} - V_{TH}) \qquad \text{Equation (9)}$$

Thus the inverter transfer function is thus found to be

$$V_{out} = VDD - GV_{in} + V_{TH}(G-1) \qquad \text{Equation (10)}$$

where *G*, the gain, is given by

$$G = Z_\alpha / Z_\beta \qquad \text{Equation (11)}$$

The SFET are designed so that the gain is greater than unity, a necessary requirement for a well behaved inverter. From now on it is assumed that G is greater than unity.

The transfer function of three examples of the inverter is shown in Figures 6, 7, and 8.

These figures all show the output, V_{out} , along the axis labeled 22, as a function of the input voltage, V_{in} , along the axis labeled 23. The transfer function is the line labeled 24. These figures all contain a region which follows Equation (10).

Consider now the inverter behavior at large input voltage. Here the assumptions of Equation (5), used to derive the linear fall of Equation (10), break down when the inverter output falls below V_T . Then the αSFET has a small source - drain voltage, but a large source gate - voltage, and behaves according to Equation (6). The resulting behavior is shown in Figures 6, 7 and 8.

When the input voltage falls below ($V_{TH} + V_T$) the αSFET follows Equation (7). The current is constant, and so then is the output voltage. If ($V_{TH} + V_T$) <0, then this domain of behavior is not reached; the transfer function is as Equation (10) down to the smallest input voltages. These two possibilities are seen in Figures 6, 7 and 8.

The Figures 6, 7, and 8 are drawn to scale for different inverter parameters, as given by Table (1).

Figure	Supply voltage, *VDD* millivolts	V_T millivolts	Gain G	Threshold Voltage, V_{TH} millivolts
6	1000	25	2	-30
7	200	25	2	25
8	100	25	1.5	-30

Table (1). Inverter Parameters.

The Figures 6, 7 and 8 also show two conjugate points, labeled 25 and 26. These have the property that

$V_{in}\,(25) = V_{out}\,(26) = Low$

$V_{in}\,(26) = V_{out}\,(25) = High$

where we have introduced *High* and *Low* to denote the voltages of the conjugate points. Consider a sequence of inverters, (1, 2, 3 .....*n*,….), connected in series. The conjugate points have the property that if the output of *n* is in state *High*, then the output of (*n* + 1) is in state *Low*, and the output of (*n* + 2) is in state *High*. In particular, a voltage pulse, switching between voltage levels *High* and *Low*, will propagate unchanged along the sequence.

Thus, Boolean logic circuits can be built from such inverters.

Figure 6 shows that, for a large supply voltage of 1000 mV, then *High* and *Low* are well separated, and close to *VDD* and zero respectively. On reducing the supply voltage to 200 mV, as in Figure 7, *High* and *Low* are still clearly defined. However, having clear and well separated *High* and *Low* states becomes more difficult as the supply voltage is further reduced to 100 mV, as in Figure 8.

The limit on the supply voltage reduction, desirable for low energy consumption, is due to fundamental statistical physics, giving the inevitable Boltzmann distribution of solectron energies under the source and drain

6 Claims

1. A field effect transistor in which the current carrier in the source - drain channel is an electron solectron which is a coherent particle formed from an electron and accompanying lattice distortion.

2. A field effect transistor in which the current carrier in the source - drain channel is a hole solectron which is a coherent particle formed from a hole and accompanying lattice distortion.

3. An inverter constructed from the field effect transistors of claim 1.

7 Abstract

A solectron field effect transistor (SFET) is described in which the current carrier is a solectron.

The SFET can work with a sub nanosecond response time. Compared to the silicon FET, the SFET can work at lower current, at smaller supply voltages, and has a smaller output impedance, and a smaller input capacity.

An inverter is described, made from two such SFET which can work with a sub nanosecond response time. Compared to an inverter made from two silicon FET, the SFET inverter can work at lower supply voltage, lower current, and at lower switching energy than the corresponding silicon FET.

The SFET can reduce the energy consumption of computation, and of electronic communication devices.

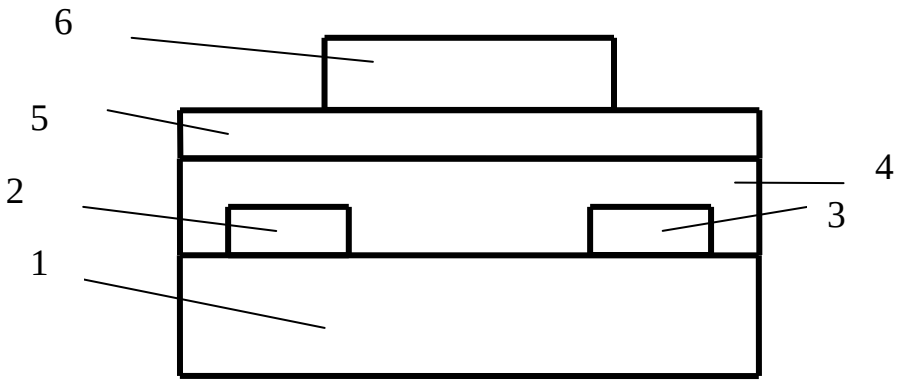

FIGURE 1

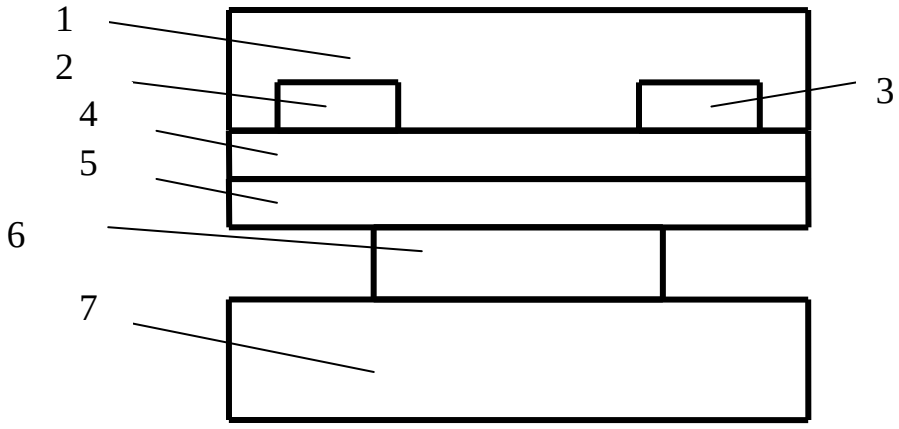

FIGURE 2

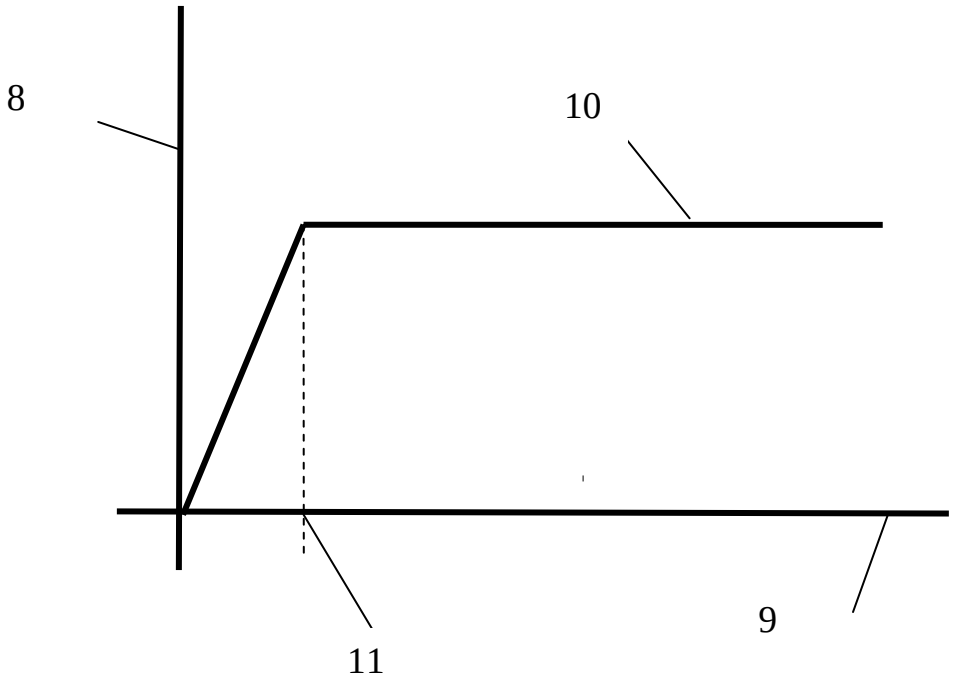

FIGURE 3

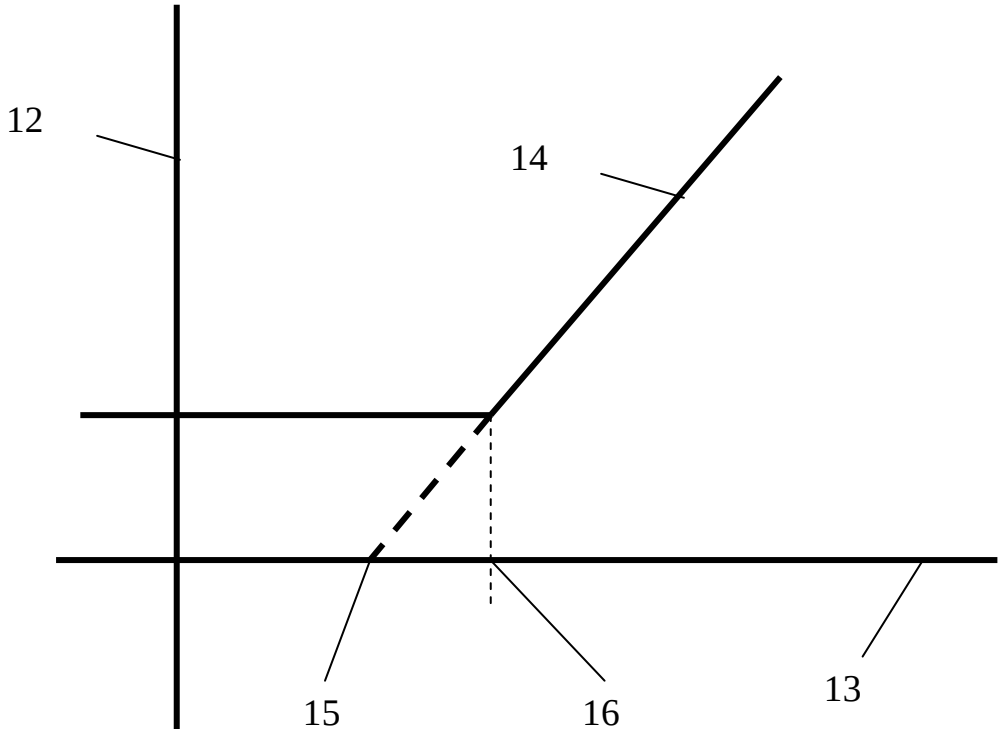

FIGURE 4

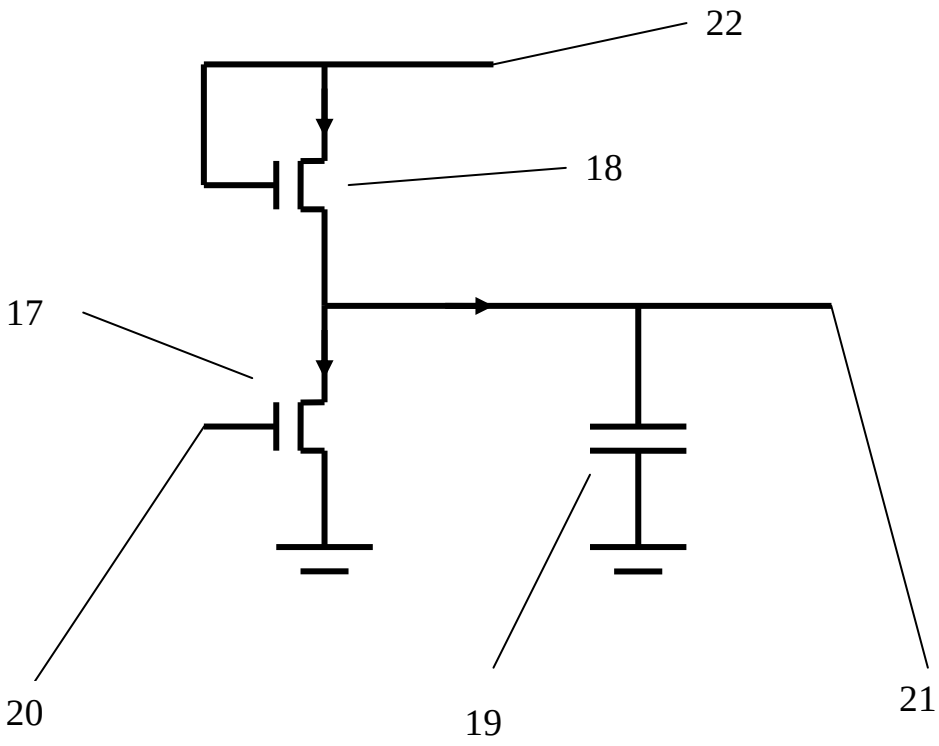

FIGURE 5

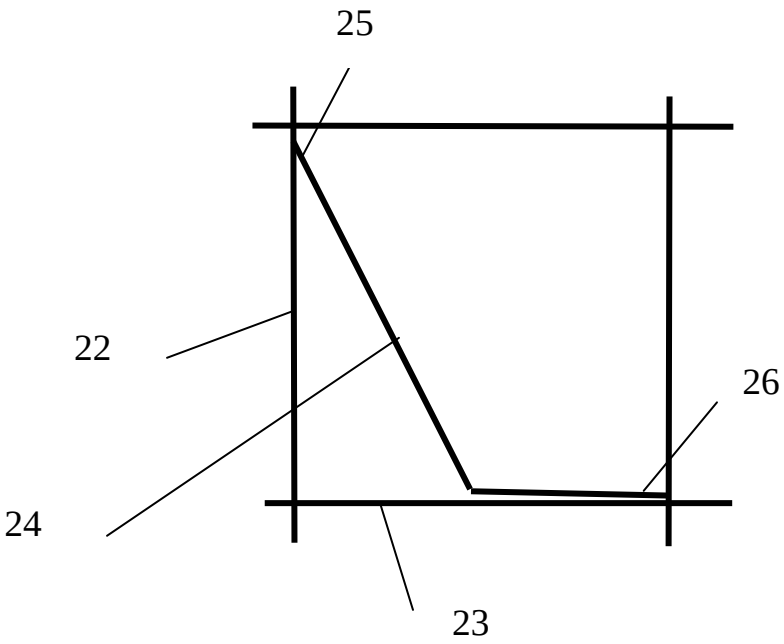

FIGURE 6

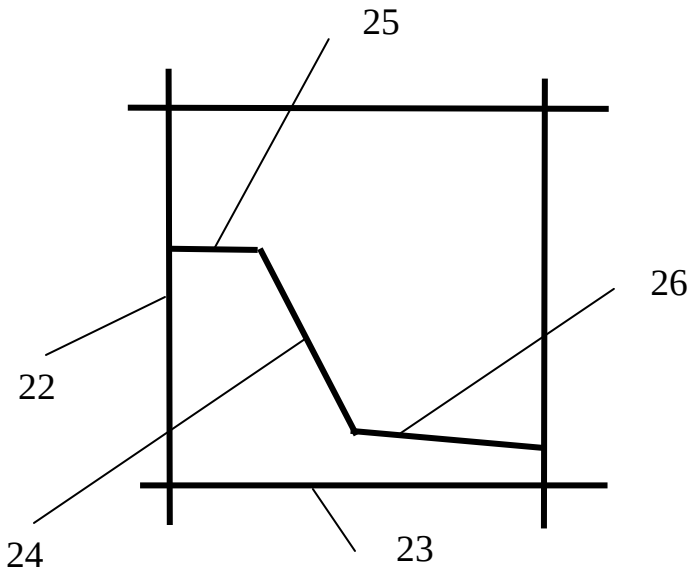

FIGURE 7

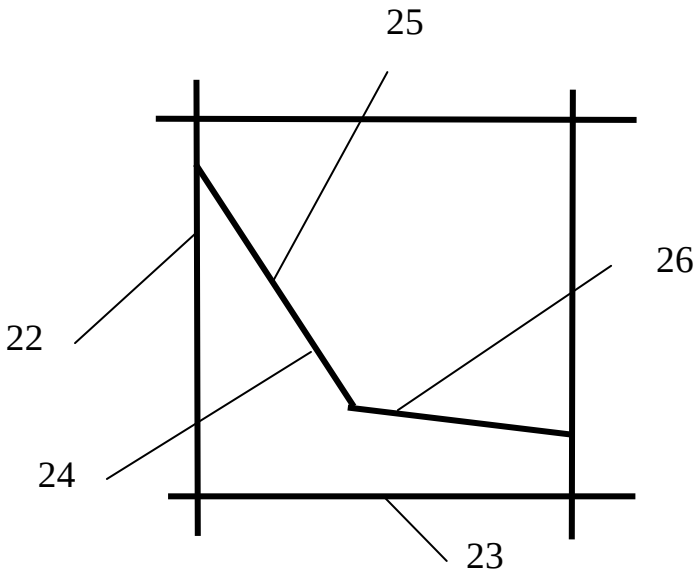

FIGURE 8